

REMARKSClaim Rejections Under 35 U.S.C. § 112

Claims 5 and 9-11 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 5 and 9 have been amended to overcome the rejection under 35 U.S.C. § 112, second paragraph.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 5, 7, 9-11, 16 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Hirano* (U.S. Patent No.6,714,459). Applicants respectfully traverse this rejection.

Claims 1, 9, 16, and 20 have been amended to more clearly claim additional subject matter that Applicants regard as part of the invention. Both claims have included limitations that the erase pulses are generated without first performing a preprogram step. This added limitation is fully supported in multiple locations of the specification including paragraphs 19 and 43.

*Hirano* discloses a non-volatile semiconductor memory and method for detecting an overerased cell. The method is comprised of performing a program before the erase (S1), verifying the program before the erase (S2), applying an erase pulse (S3), performing an erase verify (S4), and detecting an overerased cell (S5) (see Figure 3 and col. 12, lines 13 – 18). *Hirano* not only neither teaches nor suggests Applicants' invention, as claimed in the amended claims, but *Hirano* actually teaches away from Applicants' invention.

Applicants' amended claims are to generating an erase pulse, without the need for a preprogram step, then detecting any overerased cells and performing a soft program operation on the cells. The present specification (paragraphs 19 and 43) states that this greatly reduces the time required to perform an erase operation and provides for a better erase cell current distribution than possible with the method disclosed in *Hirano*. *Hirano* requires the additional time of both a preprogram step and a verify of the preprogram operation prior to applying an erase pulse. This is the problem that Applicants' invention fixes.

Claim Rejections Under 35 U.S.C. § 103

Claims 8, 18, 20, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hirano* (U.S. Patent No. 6,714,459) in view of *Joo* (U.S. Patent No.6,504,765) and *Moarotta* (U.S. Publication No. 2003/0053348). Applicants respectfully traverse this rejection.

**RESPONSE TO NON-FINAL OFFICE ACTION**

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Title: MEMORY BLOCK ERASING IN A FLASH MEMORY DEVICE

Attorney Docket No. 400.242US01

It was shown above that *Hirano* teaches away from Applicants' invention as claimed in the amended claims. Therefore, even if it were obvious to combine *Hirano* with either *Joo* and/or *Moarotta*, and Applicants maintain that it is not, the combination would not anticipate Applicants' invention.

**Allowable Subject Matter**

Claims 2-4, 6 and 19 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Claims 12-15 and 22-24 were allowed.

**CONCLUSION**

For the above-cited reasons, Applicants respectfully request that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: 6/21/05

  
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